CLAIM LISTING

1. (Currently Amended) A system for displaying images on a display, said system comprising:

a decoder for decoding encoded images and parameters associated with the images;

image buffers for storing the decoded images;

parameter buffers for storing the decoded parameters associated with the decoded images;

a display manager for determining when to overwrite an existing image in the image buffers, wherein determining when to overwrite the existing image further comprises determining when the existing image has finished display for the last time and is no longer needed for decoding other images, and providing a signal to the decoder indicating when to overwrite the existing image in the image buffer; and

wherein the decoder overwrites the existing image after receiving the signal; and

wherein the decoded images are provided for display in the forward order at normal speed.

2. (Original) The system according to claim 1 wherein the set of parameters includes a parameter indicating when the system is utilizing a technique requiring selective images to be displayed more than once.

3. (Original) The system according to claim 1 wherein the system further comprises:

a first processor;

a second processor;

a first memory;

a second memory; and

wherein the first memory stores an instruction set for the decoder.

4. (Original) The system according to claim 3 wherein the first processor executes the instruction set for the decoder.

5. (Original) The system according to claim 4 wherein the second memory stores an instruction set for the display manager, the instruction set for the display manager executed by the second processor.

6. (Original) The system according to claim 5 wherein the second processor determines when to overwrite the existing image.

7. (Original) The system according to claim 6 wherein an integrated circuit comprises the first processor and first memory, and wherein the second processor is off-chip from the integrated circuit.

8. (Original) The system according to claim 3 wherein the second memory is an off-chip memory.

9. (Original) The system according to claim 3 wherein the first memory is a SRAM.

10. (Original) The system according to claim 3 wherein the second memory is a DRAM.

11. (Original) The system according to claim 3 wherein the second memory stores the image buffers.

12. (Original) The system according to claim 3 wherein the second memory stores the parameter buffers.

13. (Currently Amended) A circuit for displaying images on a display, said circuit comprising:

a first processor; and

a first memory connected to the processor, the first memory storing instructions, wherein execution of the instructions by the first processor causes:

decoding images; and

overwriting an existing image after the processor receives a signal indicating when to overwrite the existing image, wherein indicating when to overwrite the existing image further comprises determining when the existing image has finished display for the last time and is no longer needed for decoding other images; and

wherein at least some of the pictures are stored for at least one display period after the at least some of the pictures are displayed.

14. (Original) The circuit of claim 13, wherein execution of the instructions by the first processor further causes:

displaying the images.

15. (Original) The circuit of claim 13, further comprising:

a second processor connected to the integrated circuit; and

a second memory connected to the processor, the second memory storing instructions, wherein execution of the instructions by the second processor causes:

determining when to overwrite the existing frame; and

transmitting the signal to the first processor indicating when to overwrite the existing frame.

16. (Original) The circuit of claim 15, wherein execution of the instructions in the first memory by the first processor further causes:

decoding parameters associated with the images.

17. (Original) The circuit of claim 16, wherein determining when to overwrite the existing frame further comprises:

examining some of the decoded parameters associated with the images by the second processor.

18. (Original) The circuit of claim 16, further comprising a parameter buffer connected to the integrated circuit and a frame buffer connected to the integrated circuit, wherein the parameter buffer stores the decoded parameters, and the frame buffer stores the decoded images.

19-21. (Cancelled)

22. (Previously Presented) The circuit of claim 1, wherein the display manager determines when to overwrite an existing image in the image buffer based at least in part on at least one of the decoded parameters.

23. (Previously Presented) The circuit of claim 2, wherein the display manager determines when to overwrite an existing image based on the parameter indicating when the system is utilizing the technique requiring selective images to be displayed more than once.

24. (Previously Presented) The circuit of claim 1, wherein the display manager determine when to overwrite an existing image with another image, wherein the another image and the existing image are from a same video sequence.